WHAT IS CLAIMED IS:

1. A method of forming a semiconductor varactor device having improved linearity comprising the steps of:

providing a semiconductor substrate;

forming at least a first and a second differential varactor element on said semiconductor substrate, the forming of each of said differential varactor elements comprising the steps of forming first, second and third N+ doped regions in an N well, forming a first gate for controlling said first and second N+ doped regions and forming a second gate for controlling said second and third N+ doped regions;

connecting said first, second and third N+ doped regions of said first differential varactor element to receive power having a first voltage; and

connecting said first, second and third N+ doped regions of said second differential varactor element to receive power having a second voltage different than said first voltage.

2. The method of claim 1 further comprising forming a first resistor in said semiconductor varactor device connected to receive power from a voltage source, and wherein said step of connecting said first, second and third N+ doped regions of said first differential varactor comprises connecting to said voltage source, and wherein said step of connecting said first, second and third N+ doped regions of said second differential varactor comprises connecting to said voltage source through said first resistor.

3. The method of claim 1 wherein said step of forming said first and second gates comprises the step of forming a first N-type gate and forming a second N-type gate.

4. The method of claim 2 wherein said step of forming a first resistor comprises the step of forming another resistor and said first resistor and wherein said another resistor is connected in series and between said voltage source and said first resistor, wherein said step of connecting said first, second and third N+ doped regions of said first differential varactor element to receive power from said voltage source comprises the step of connecting said regions to said voltage source through said another resistor, and such that said second differential varactor elements receive power from said voltage source through both of said another and said first resistors.

5. The method of claim 2 wherein said step of forming at least a first and a second differential varactor element comprises the step of forming at least a first, a second and a third differential varactor element, wherein said step of forming a first resistor comprises the step of forming first and second resistors connected in series and further comprising the step of connecting said first, second and third N+ doped regions of said third differential varactor element to receive power from said voltage source through both of said first and second resistors.

6. The method of claim 5 wherein said step of forming first and second resistors comprises the step of forming another resistor and said first and second resistors and wherein said another resistor is connected in series between said voltage source and said first and second resistors and wherein said step of connecting said first, second and third N+ doped regions of said first differential varactor element to receive power from said voltage source comprises the step of connecting said voltage source to said regions only through said another resistor.

7. The method of claim 2 wherein said step of forming first and second differential varactor elements comprises the step of forming a plurality of differential varactor elements, wherein said step of forming a first resistor comprises the step of forming a plurality of resistors connected in

series such that nodes are defined between adjacent ones of said serially connected plurality of resistors and further comprising the step of connecting said first, second and third N+ doped regions of one each of said plurality of differential varactor elements to one each of said nodes such that said first, second and third N+ doped regions of different ones of said plurality of differential varactor elements are electrically separated by one of said plurality of resistors.

8. The method of claim 7 wherein said step of forming a plurality of resistors further comprises the step of forming said plurality of resistors and another resistor and connecting said another resistor in series between said voltage source and said serially connected plurality of resistors and wherein said step of connecting said first differential varactor element to receive power from said voltage source comprises the step of connecting said voltage source to said varactor element through said another resistor.

9. The method of claim 1 further comprising the steps of connecting said first gate of said first and second differential varactor elements together at a first terminal and connecting said second gate of said first and second differential varactor elements together at a second terminal.

10. The method of claim 5 further comprising the steps of connecting said first gate of said first, second and third differential varactor elements together at a first terminal and connecting said second gate of said first, second and third differential varactor element together at a second terminal.

11. The method of claim 7 further comprising the steps of connecting said first gate of said plurality of differential varactor elements together at a first terminal and connecting said second gate of said plurality of differential varactor elements together at a second terminal.

12. The method of claim 9 further comprising connecting said first and second terminals to an oscillator circuit as a voltage controlled capacitor.

13. The method of claim 11 further comprising connecting said first and second terminals to an oscillator circuit as a voltage controlled capacitor.

14. The method of claim 1 wherein said forming steps are according to a CMOS process.

15. The method of claim 9 wherein said first and second gates are N-type gates.

16. The method of claim 10 wherein said first and second gates are N-type gates.

17. The method of claim 11 wherein said first and second gates are N-type gates.

18. The method of claim 1 further comprising the steps of forming another differential varactor element on said semiconductor, said another differential varactor element comprising first, second and third P+ doped regions in a P well, a first gate for controlling said first and second P+ doped regions and a second gate for controlling said second and third P+ doped regions, and connecting said first, second and third P+ doped regions to receive power from said voltage source.

19. The method of claim 2 wherein said step of forming a first resistor comprises the step of forming said first resistor from a polysilicon material.

20. A semiconductor varactor device having improved linearity and suitable for being manufactured by a standard CMOS process comprising:

a semiconductor substrate;

at least two N wells formed in said semiconductor substrate;

first, second and third N+ doped regions formed in each of said at least two N wells;

a first gate connected to a first junction and formed between said first and second N+ doped regions of a first one of said at least two N wells, and a first gate connected to said first junction and formed between said first and second N+ doped regions of the other one of said at least two N wells;

a second gate connected to a second junction and formed between said second and third N+ doped regions of said first one of said at least two N wells and a second gate connected to said second junction and formed between said second and third N+ doped regions of said other one of said at least two N wells; and

a power source for providing a first voltage level and a second voltage level, said power source connecting said first resistor and said first, second and third N+ doped regions formed in said first one of said at least two N wells to receive power having said first voltage level and connecting said first, second and third N+ doped regions formed in said second one of said at least two N wells to receive power having said second voltage level.

21. The semiconductor varactor of claim 20 wherein said first voltage level is the output of said power source, and further comprising a first resistor formed on said semiconductor substrate and having a first end and a second end, said first end connected to the output of said power source and said second end connected to said first, second and third N+ doped regions formed in said second of said at least two N wells to provide said second voltage level.

22. The semiconductor varactor of claim 20 wherein said first and second gates are N-type gates.

23. The semiconductor varactor of claim 21 further comprising another resistor connected in series with said first resistor, said another resistor further connected between said voltage source and said first resistor such that said first, second and third N+ doped regions formed in said first one of said at least two N wells receives power from said voltage source through said another resistor.

24. The semiconductor varactor of claim 21 wherein said at least two N wells comprise at least three N wells and further comprising another first gate connected to said first junction and formed between said first and second N+ doped regions of the third one of said at least three N wells, another second gate connected to said second junction and formed between said second and third N+ doped regions of the third one of said at least three N wells, a second resistor connected in series with said first resistor and said first, second and third N+ doped regions of the third one of said at least three N wells connected to receive power from said voltage source through said first and second resistors.

25. The semiconductor varactor of claim 24 further comprising another resistor connected in series with said first and second resistor, said another resistor further connected between said voltage source and said first resistor such that said first, second and third N+ doped regions formed in said first one of said at least three N wells receives power from said voltage source through said another resistor.

26. The semiconductor varactor of claim 21 wherein said at least two N wells comprise a plurality of N wells, and further comprising a plurality of first gates connected to said first junction and formed between said first and second N+ doped regions of said plurality of N wells, a plurality of second gates connected to said second junction and formed between said second and third N+ doped region of said plurality of N wells, a plurality of resistors connected in series such that nodes are defined between two adjacent ones of said plurality of resistors, and wherein said first, second and third N+ doped regions of each one of said plurality of N wells are connected to one each of said nodes such that said first, second and third N+ doped regions of each one of said plurality are electrically separated by one of said plurality of resistors.

27. The semiconductor varactor of claim 26 further comprising another resistor connected in series with said plurality of resistors, said another resistor further connected between said voltage source and said plurality of resistors such that said first, second and third N+ doped regions formed in said first one of said plurality of N wells receive power from said voltage source through said another resistor.

28. The semiconductor varactor of claim 21 further comprising circuitry for forming an oscillator circuit when connected with said semiconductor varactor, said first and second junctions of said varactor device connected such that said semiconductor varactor operates as a voltage controlled capacitor of said oscillator circuit.

29. The semiconductor varactor of claim 20 wherein said first resistor is made of a polysilicon material.

30. The semiconductor varactor of claim 20 further comprising a P well formed in said semiconductor substrate and first, second and third P+ doped regions formed in said P well, a first gate for controlling said first and second P+ doped regions and a second gate for controlling said second and third P+ doped regions, said first, second and third P+ doped regions connected to receive power from said voltage source.